IN THE CLAIMS:

Please cancel claim 19. **Please also amend** claims 1 and 2as shown in the complete list of claims that is presented below.

1. (currently amended) A receiver apparatus comprising:

a demodulator for demodulating received radio signals into digital signals;

a mode selector for selecting either of a reproduction mode of reproducing the digital signals and an evaluation mode of evaluating the digital signals; and

an error generator for inverting a level of the digital signals for the evaluation mode at a predetermined timing to generate error [[data.]] data,

wherein said mode selector comprises a pair of single pole, double throw switches that are connected to one another, both switches being responsive to a common selection signal.

2. (currently amended) The apparatus in accordance with claim 1, wherein said mode selector comprises:

a first selector switch for selecting a destination of the digital signals; and

a second selector switch for selecting a source from either of said first selector and said error generator;

said first and second ~~selectors~~ selector switches synchronously selecting a same mode side.

3. (original) The apparatus in accordance with claim 2, wherein said error generator comprises:

a pulse outputting circuit for outputting pulse signals at the predetermined timing; and

an inverter for inverting the level of the digital signals responsive to a transmission of the pulse signals.

4. (original) The apparatus in accordance with claim 3, wherein said error generator comprises a preset value holding circuit which has a preset value defining a transmission timing of the pulse signals set from outside said apparatus to hold the preset value to supply the preset value to said pulse outputting circuit.

Claims 5 and 6 (cancelled).

7. (original) The apparatus in accordance with claim 3, further comprising an error detector interconnected to said mode selector for detecting an error contained in the digital signals;

said error detector supplying said pulse outputting circuit with an output timing defining a field of the digital signal in which check data for received data are held.

8. (original) The apparatus in accordance with claim 4, further comprising an error detector interconnected to said mode selector for detecting an error contained in the digital signals;

said error detector supplying said pulse outputting circuit with an output timing defining a field of the digital signal in which check data for received data are held.

Claims 9 and 10 (cancelled).

11. (previously presented) The apparatus in accordance with claim 3, further comprising a sync pattern detector interconnected to said mode selector for detecting a sync pattern contained in the digital signals;

said sync pattern detector supplying said pulse outputting circuit with an output timing defining a field of received data which follows the sync pattern and holds check data.

12. (previously presented) The apparatus in accordance with claim 4, further comprising a sync pattern detector interconnected to said mode selector for detecting a sync pattern contained in the digital signals;

said sync pattern detector supplying said pulse outputting circuit with an output timing defining a field of received data which follows the sync pattern and holds check data.

Claims 13, 14, and 15 (cancelled).

16. (original) The apparatus in accordance with claim 11, further comprising:

an error detector for detecting an error contained in the digital signals; and

a timing selector for selecting an output timing supplied from either of said error detector and said sync pattern detector.

17. (original) The apparatus in accordance with claim 12, further comprising:

an error detector for detecting an error contained in the digital signals; and

a timing selector for selecting an output timing supplied from either of said error detector and said sync pattern detector.

Claim 18-19 (cancelled).